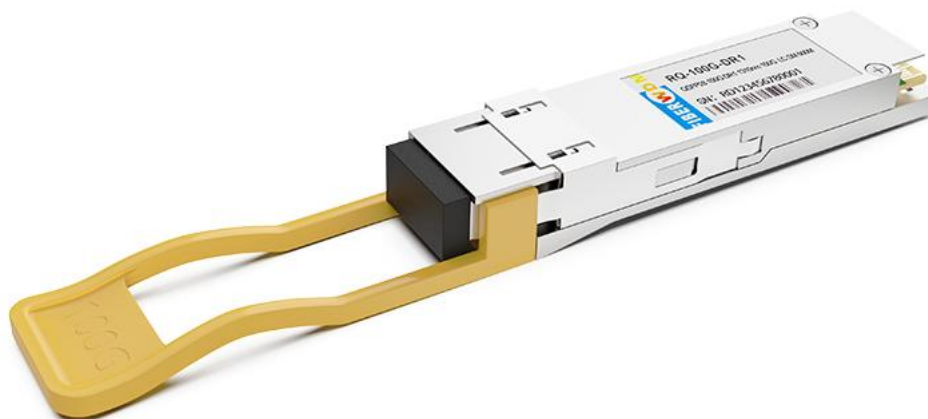


RQ-100G-DR1

100G QSFP28 DR1 1310nm LC SM 500M



The 100G QSFP28 DR1 Transceiver is designed to transmit and receive serial optical data links up to 106.25Gb/s data rate by PAM4 modulation format over single-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with the EML laser. It is compliant with 100G Lambda MSA, QSFP MSA.

Features

- ◆ Up to 106.25Gbps data rate by PAM4 modulation
- ◆ 1x100G PAM4 EML laser
- ◆ Duplex LC receptacle optical interface
- ◆ Single +3.3V power supply
- ◆ DDM function implemented
- ◆ Hot-pluggable QSFP28 form factor
- ◆ Maximum link length of 500m on SMF fiber
- ◆ Low power dissipation: <3.5W
- ◆ International class 1 laser safety certified
- ◆ Operating temperature range: 0°C ~ +70 °C
- ◆ Compliant with ROHS6.0

Applications

- ◆ 100GBASE Ethernet Links
- ◆ Switch & Router Connections
- ◆ Data Centers

Standards

- ◆ IEEE 802.3bm
- ◆ IEEE 802.3cd
- ◆ 100G Lambda MSA
- ◆ QSFP MSA
- ◆ SFF-8636

Document History

VER. & STATUS	DATE	DESCRIPTION OF CHANGE	Modifier
1.0	2021-12-10	Draft	XY

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter (per Lane)						
Signaling Speed per Lane		GBd		53.125±100pm		
Modulation format				PAM4		
Center wavelength		nm	1304.5	1311	1317.5	
Side-mode suppression Ratio	SMSR	dB	30			
Optical output power	P _{AVG}	dBm	-2.9		4	
Outer Optical Modulation Amplitude	OMA _{outer}	dBm	-0.8		4.2	
Launch power in OMA _{outer} minus TDECQ, each lane (min): for extinction ratio ≥ 5 dB		dBm	-2.2			
Launch power in OMA _{outer} minus TDECQ, each lane (min): for extinction ratio < 5 dB		dBm	-1.9			
Transmitter and dispersion penalty eye closure for PAM4	TDECQ	dB			3.4	
Average Launch Power of Off Transmitter		dBm			-15	
Optical Extinction Ratio	ER	dB	3.5			
RIN _{17.1OMA}		dB/Hz			-136	
Optical Return Loss Tolerance	ORL	dB			15.5	
Transmitter transition time (max)		ps			17	
Transmitter reflectance		dB			-26	
Receiver(per Lane)						
Signaling Speed per Lane		GBd		53.125±100pm		
Modulation format				PAM4		
Input Operating Wavelength		nm	1304.5	1311	1317.5	
Damage threshold		dBm	5			
Average receive Power per Lane		dBm	-5.9		4	
Receive Power (OMA _{outer})		dBm			4.2	
Receiver reflectance (max)		dBm			-26	

Stressed Receiver Sensitivity (OMA _{outer})		dBm			-1.9	
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Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
RQ-100G-DR1	QSPF28	100G	EML	-2.9~4dBm	PD	Max(-3.9,SEC Q-5.3)dBm	0~70 °C	500m	RoHS	100G Base Ethernet

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	T _s	°C	-40	+85
Relative Humidity	RH	%	0	85
Power Supply Voltage	V _{cc}	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	T _c	°C	0	/	70
Power Supply Voltage	V _{cc}	V	3.135	3.3	3.465
Bit Rate(Per channel)	BR	Gbps		53.125	

Optical Interface

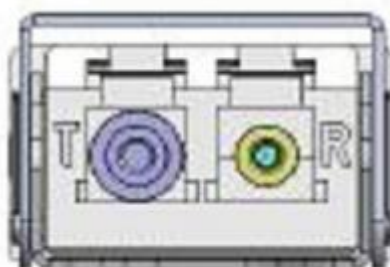


Figure 1. Optical Interface

Note: Optical interface is duplex LC.

Principle diagram

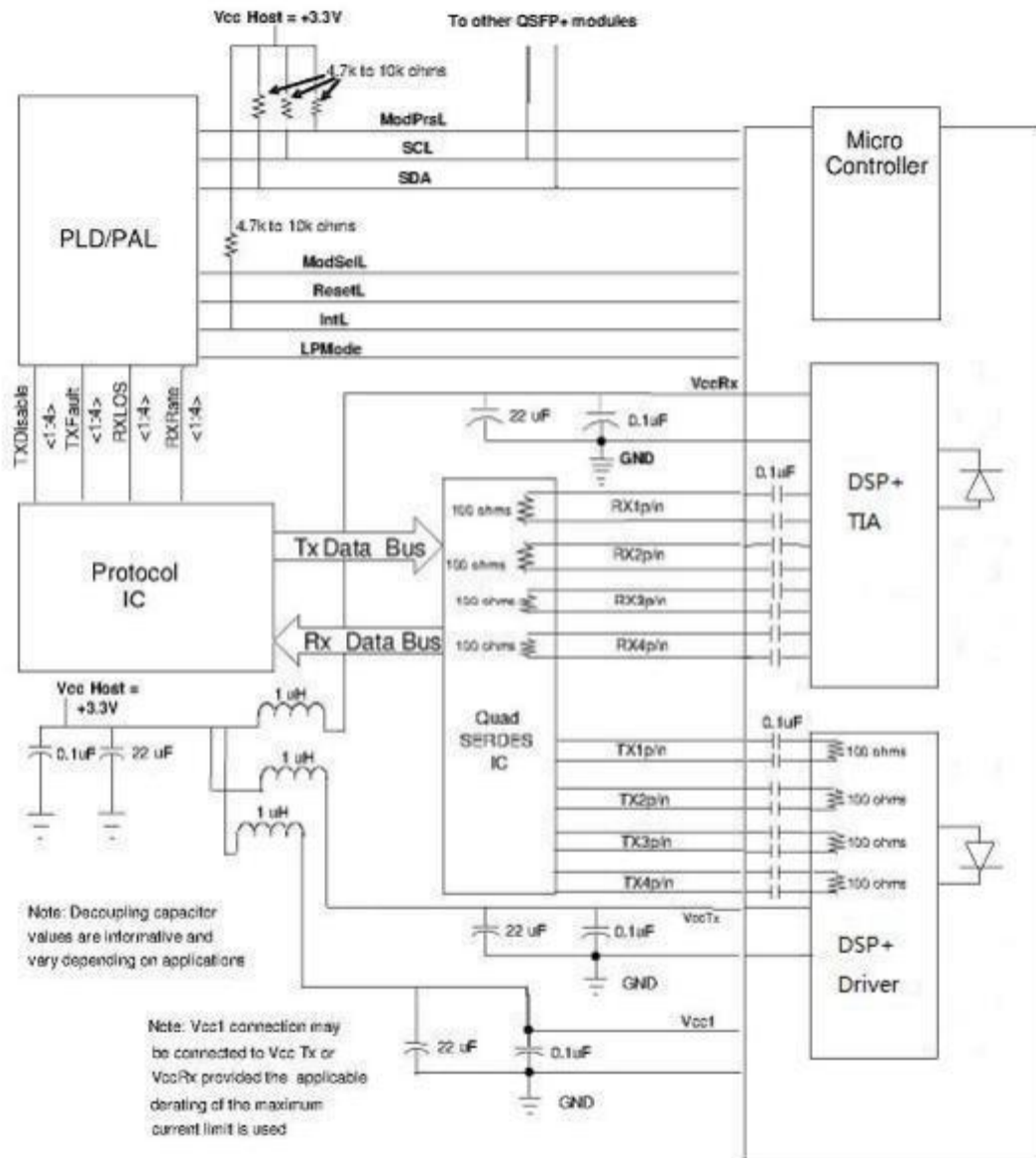


Figure 2. Module Principle Diagram

Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	V _{CC}	V	3.14		3.47	
Supply Current	I _{CC}	mA			1100	
Transmitter						
Data Rate	BR	GBd		25.78125		NRZ
TX_DISABLE High	V _{DH}	V	2		3.5	Input Voltage High
TX_DISABLE Low	V _{DL}	V	-0.3		0.8	Input Voltage Low
TX_FAULT High [assert]	V _{FH}	V	2		3.5	Output Voltage High
TX_FAULT Low [negated]	V _{FL}	V	-0.3		0.8	Output Voltage Low

Receiver						
Data Rate	BR	GBd		25.78125		NRZ
Differential Output Swing	V_{RXDIFF}	mV	400		800	At TP4
Differential Eye Height	V_{EH}	mV	228			
Los-Output Voltage High	V_{OH}	V	2		3.5	Output Voltage High
Loss-Output Voltage Low	V_{OL}	V	-0.3		0.8	Output Voltage Low

Pin Description

No	Pin	Definition	Description	Note
1	1	GND	Ground	1
2	2	Tx2n	Transmitter Inverted Data Input	
3	3	Tx2p	Transmitter Non-Inverted Data Input	
4	4	GND	Ground	1
5	5	Tx4n	Transmitter Inverted Data Input	
6	6	Tx4p	Transmitter Non-Inverted Data Input	
7	7	GND	Ground	1
8	8	ModSelL	Module Select	
9	9	ResetL	Module Reset	
10	10	VccRx	+3.3V Power Supply Receiver	2
11	11	SCL	2-wire serial interface clock	
12	12	SDA	2-wire serial interface data	
13	13	GND	Ground	1
14	14	Rx3p	Receiver Non-Inverted Data Output	
15	15	Rx3n	Receiver Inverted Data Output	
16	16	Ground	Ground	1
17	17	Rx1p	Receiver Non-Inverted Data Output	
18	18	Rx1n	Receiver Inverted Data Output	
19	19	GND	Ground	1
20	20	GND	Ground	1
21	21	Rx2n	Receiver Non-Inverted Data Output	
22	22	Rx2p	Receiver Inverted Data Output	
23	23	Ground	Ground	1
24	24	Rx4n	Receiver Non-Inverted Data Output	
25	25	Rx4p	Receiver Inverted Data Output	
26	26	Ground	Ground	1
27	27	ModPrsL	Module Present	
28	28	IntL	Interrupt	
29	29	VccTx	+3.3V Power supply transmitter	2
30	30	Vcc1	+3.3v Power supply	2
31	31	LPMODE	Low Power Mode	

32	32	GND	Ground	1
33	33	Tx3p	Transmitter Non-Inverted Data Input	
34	34	Tx3n	Transmitter Inverted Data Input	
35	35	GND	Ground	1
36	36	Tx1p	Transmitter Non-Inverted Data Input	
37	37	Tx1n	Transmitter Inverted Data Input	
38	38	GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. VccRx, Vcc1 and VccTx may be internally

connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

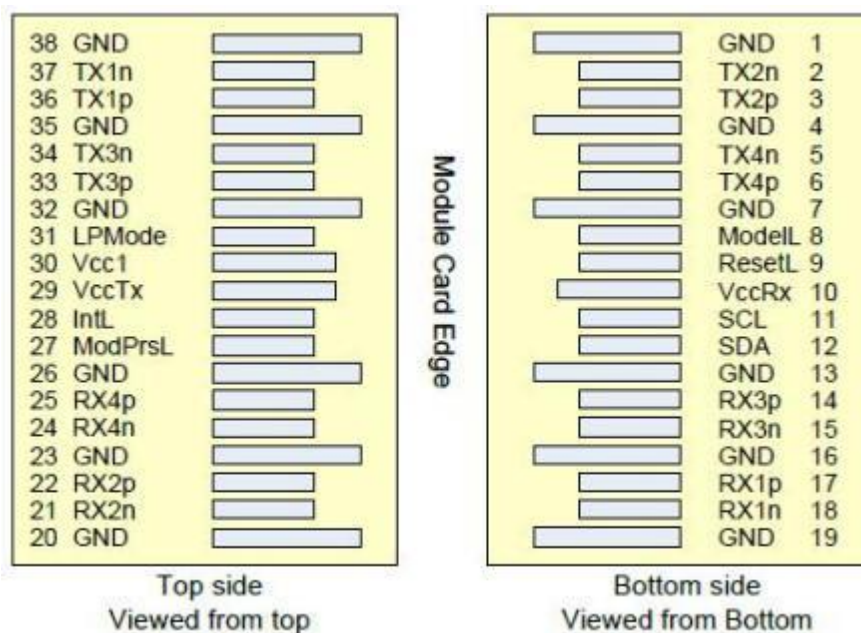


Figure 3. Electrical Pin-out Details

Module Memory Map

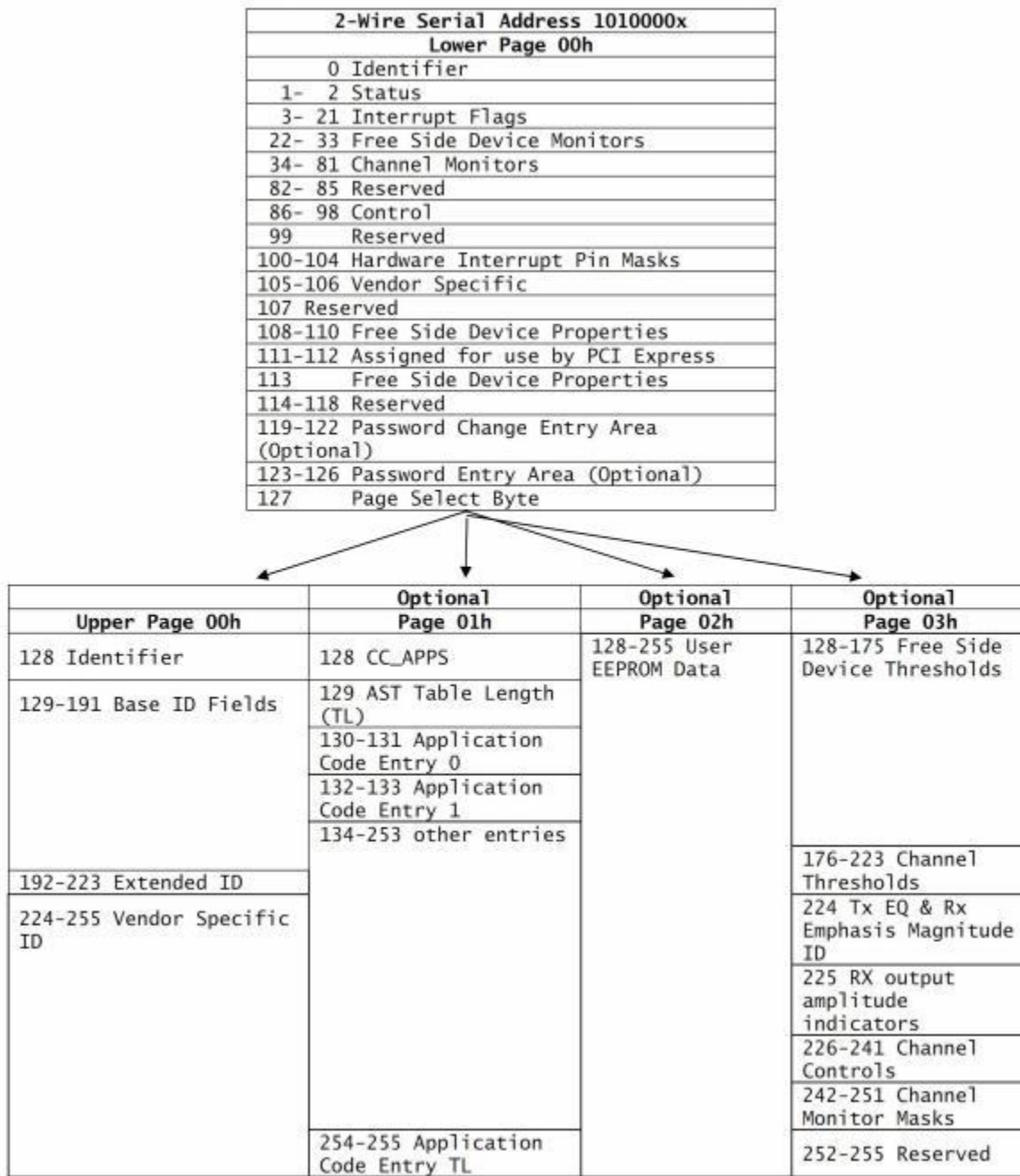


Figure 4 Digital Diagnostic Memory Map

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

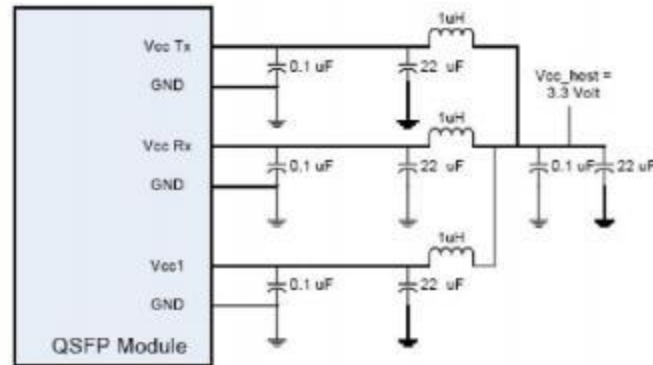


Figure 5 Recommended Host Board Power Supply Filtering

Figure 6 Package Outline

#105 ±0.05
12 PL

0.80 0.75 0.60

97.00 MAX.

22.25

17.90 REF.

CROSS-HATCHED AREA DENOTES COMPONENT AND TRACE KEEP-OUT EXCEPT CHASSIS GROUND

THIS AREA DENOTES COMPONENT KEEP-OUT (TRACES ALLOWED)

ESTABLISHED BY PROCUAL OF SURFACE OF EDGE OF PCB IS FIN

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